Wafer Sub-Layer Impact In OPC/ORC Models For Advanced Node Implant Layers

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ABSTRACT

From 28 nm technology node and below optical proximity correction (OPC) needs to take into account light scattering effects from prior layers when bottom anti-reflective coating (BARC) is not used, which is typical for ionic implantation layers. These effects are complex, especially when multiple sub layers have to be considered: for instance active and poly structures need to be accounted for.

A new model form has been developed to address this wafer topography during model calibration called the wafer 3D+ or W3D+ model. This model can then be used in verification (using Tachyon LMC) and during model based OPC to increase the accuracy of mask correction and verification. This paper discusses an exploration of this new model results using extended wafer measurements (including SEM). Current results show good accuracy on various representative structures.

Keywords: OPC, stack effect, wafer topography, optical lithography, mask verification, ionic implantation.

1. INTRODUCTION

Optical photolithography process of ionic implantation layers are becoming critical starting 2x nm nodes and below with no longer negligible unwanted optical effects induced by underlying layers. Indeed these underlying Active and Polysilicon (Rx & Poly) layers for Source and Drain (SD) Ionic implantation patterning step are the source of indirect energy absorption into the resist during optical photolithography process. This phenomenon damages drastically the ionic implantation patterning up to collapse behavior for the smallest design structures in specific sub layer configurations. The classical solution to reduce this wafer stack effect phenomenon is to add a bottom anti-reflective coating (BARC) within the optical photolithography process. However this solution increases process complexity, cycle time and cost. As a consequence, BARC usage is not the reference process retained for SD ionic implantation process step in 28 nm bulk technology. In absence of a bottom anti-reflective coating (BARC) layer, sub-layer patterns will strongly influence the optical field for an implant layer. The sub-layer pattern not only brings filmstack variations, but also reflects lights back into resist from their edges.

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Then, the alternative approach to cope with those optical effects consists in creating a model able to simulate the complex physical phenomenon induced by underlying layers during optical photolithography to predict resist contour modulation and patterning degradation. Although wafer topography effects can be simulated closely by rigorous electromagnetic field (EMF) solvers, the computational cost is too high for full-chip applications.

ASML Brion has developed an advanced physical wafer topography (W3D+) model for full-chip applications [1]. It uses a library of rigorous EM fields of representative topography features to calculate the wafer optical image on large scale. The library is pre-computed using a rigorous EMF solver, which takes into account the physical information of the topography features including filmstack thicknesses, materials and sidewall profiles. A set of W3D+ filters are extracted from the library and used for rendering full-chip wafer topography effects. This approach is similar to ASML Brion's Mask 3D solution [1, 2]. The dominant scattering effects from underlying pattern edges are captured by these W3D+ filters. Additionally, the residual scattering effect is allowed to be modeled by using terms from a kernel based empirical model [2]. Based on the implementation, this W3D+ model is more physical, accurate and predictive.

This model is built in order to be integrated into OPC flow to enhance mask verification.
In the first part of the paper, the W3D+ modeling approach by ASML Brion and resulting model form is presented. Then, the characterization of optical phenomenon due to under-layer is described through elementary structures like active and poly silicon patterns on Shallow Trench Isolation (STI) area and also the transitions between these several regions. The global W3D+ modeling results are presented in detail. The second part of the paper shows capability of such new model to predict wafer defects across full-chip due to stack effect for 28 nm Source Ionic implantation device.

2. W3D+ MODELING

2.1 W3D+ model form

W3D+ model form is as follows:

$$I = \sum_{\alpha=x,y,z} \left| \sqrt{I_{0\alpha}} + \sum_{\beta=x,y,z} S_{\alpha\beta} \sqrt{I_{inc,\beta}} \right|^2$$

Where I_{0x}, I_{0y} and I_{0z} are planar wafer image intensity components in x, y, z directions respectively, $I_{inc,x}$, $I_{inc,y}$ and $I_{inc,z}$are incident field image intensity components in x, y, z directions respectively, and $S_{\alpha\beta}$ is the topography function that represents scattering effects. This self-consistent model form has been presented in Ref. [1].

2.2 Model calibration flow

Systematic tuning process is used for calibrating physical wafer topography model. During calibration process, we use planar patterns and non-planar patterns to tune specific parameters.

Planar patterns are used to determine standard optical model parameters like defocus. Non-planar patterns are used to determine W3D+ filter related parameters and in the end all patterns are used together to determine W3D+ specific optical and resist parameters [1,2]. It is worth to note that multiple W3D+ filters are usually used for a single model to reflect the substrate variances due to etch loading effects. At this stage, the major metrology data trend will be well matched with the model simulations. During the calibration process, measurement height and layer thicknesses can be searched independently for different film stacks within certain tolerances, thereby accounting for standing wave effects arising from film stack variations.

3. MODELING RESULTS

3.1 28 nm bulk: Wafer stack effect involved on Ionic implantation process step

In this section, the data set of measurements used for model calibration and verification is introduced. This data set contains a large number of stack configurations which can be found on wafer at SD ionic implantation process step.

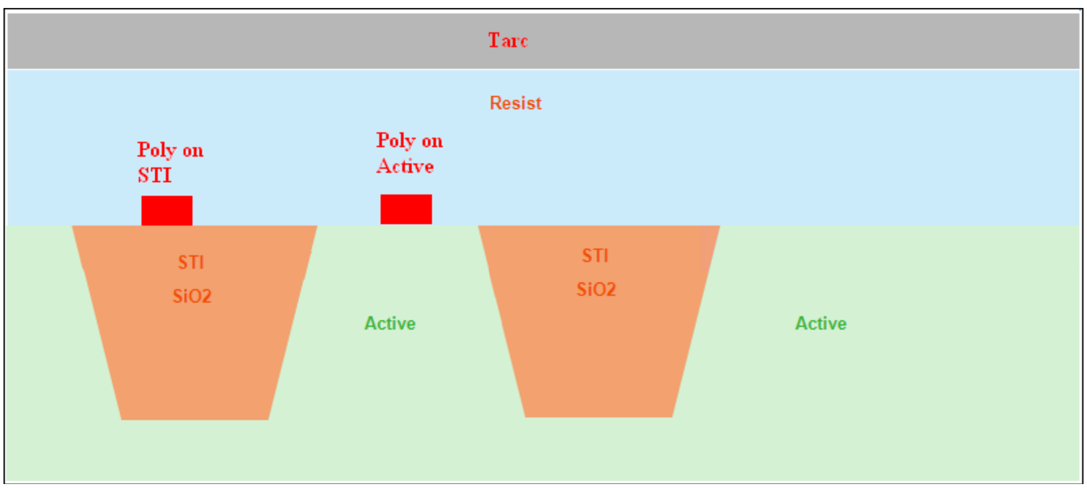


Fig.1- 28 nm bulk Source/Drain Implant stack

From stack description above (Fig1), different main stack configurations can be deduced. Indeed, resist patterns can be formed on configurations classified in the next table:

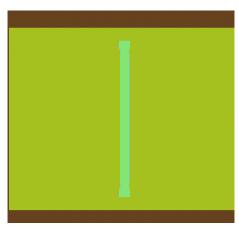
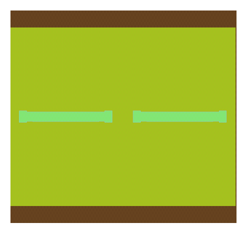
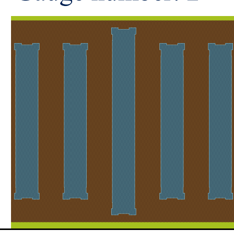
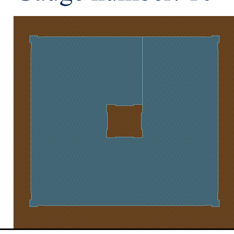
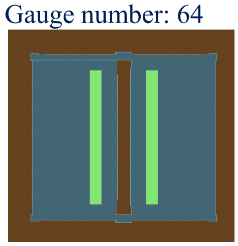
Configurations	Case	Description
One substrate only	Active substrate	The resist pattern takes place on a large active area
	STI substrate	The resist pattern takes place on a large STI area responsible for an overexposure of the resist. This effect is called STI substrate effect in this paper
Presence of	STI/Active	The resist pattern takes place on STI area with

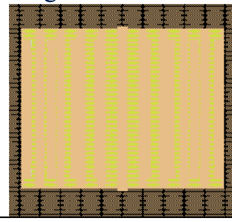
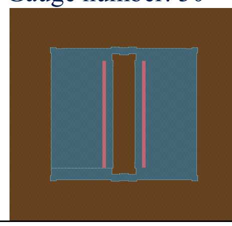
material transitions	transition	transitions between Active and STI material in the environment of the pattern
	Poly/Active transition	The resist pattern takes place on Active area with transitions between Poly and Active material in the environment of the pattern
	Poly/STI transition	The resist pattern takes place on STI area with transitions between Poly and STI material in the environment of the pattern

Tab.1- Elementary stack effect involved for 28 nm bulk Implant layer

Thus, the different configurations are Active substrate, STI substrate, Active substrate with Poly elements and STI substrate with Active or Poly elements. In addition, for each stack configuration, various resist patterns are used to evaluate the stack impact. These patterns are isolated resist lines and trenches, dense resist line arrays for 1D information, and Line end, Slot end, resist dots and holes for 2D information.

The table below gives an overview of the data used for model calibration at nominal condition:

Stack configuration	Data 1D	Data 2D
Active substrate	Gauge number: 27 	Gauge number: 12 
STI substrate	Gauge number: 2 	Gauge number: 10 
STI/Active transition	Gauge number: 64 	Gauge number: 0

Poly/Active transition	Gauge number: 198 	Gauge number: 0
Poly/STI transition	Gauge number: 30 	Gauge number: 0

Tab.2 – Data set used for model calibration.

In addition, the 1D test patterns on Active and STI substrates are measured at 5 focus conditions for optical model calibration and for Bossung trend check with more than 60 measurements by focus condition. Finally, the data set is composed by 270 structures at nominal condition and about 240 structures through defocus.

3.2 Model quality and results

In this section, the performance of FEM model, Active model and Poly model is demonstrated. The model has been calibrated to simulate the 28nm bulk implant lithography process, with 0.8 NA, 248nm wavelength, and standard illumination. It is clearly demonstrated that there is ~100 nm best focus shift between measurement data on STI substrate and on Active substrate. The simulated Bossung curve of W3D+ model captured the best focus shift reasonably well (refer to Fig 2).

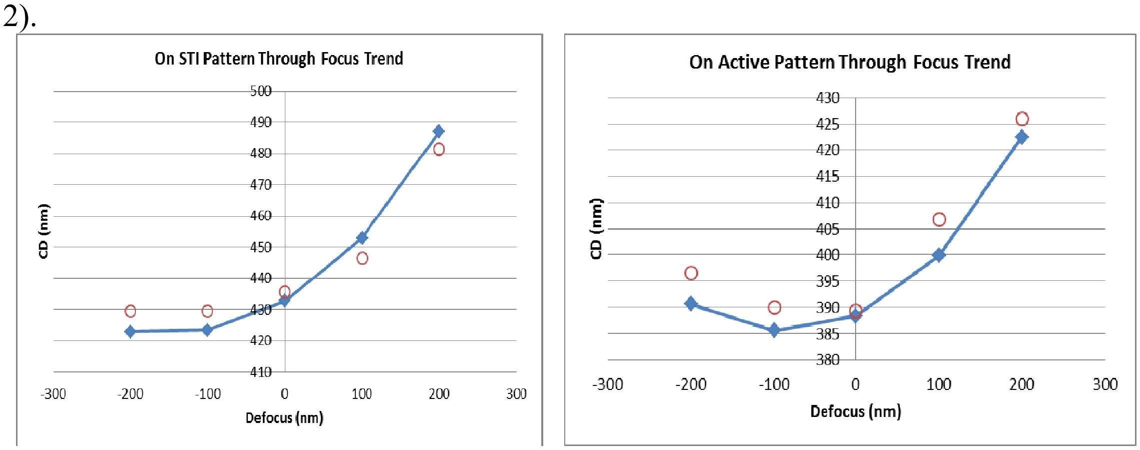


Fig 2 – Bossung plots for isolated line on STI substrate (left) and on Active substrate (right). Circles are the wafer data and blue lines are simulation result

Based on the defocus setting optimized by FEM data, W3D+ model is calibrated with edge filter related parameters. Thus all patterns planar substrate and non-planar substrate can be fitted well.

From Fig 3, the relative model error on planar substrate is mostly less than 10% and the relative model error on non-planar substrate is also limited to 10% (Fig 4).

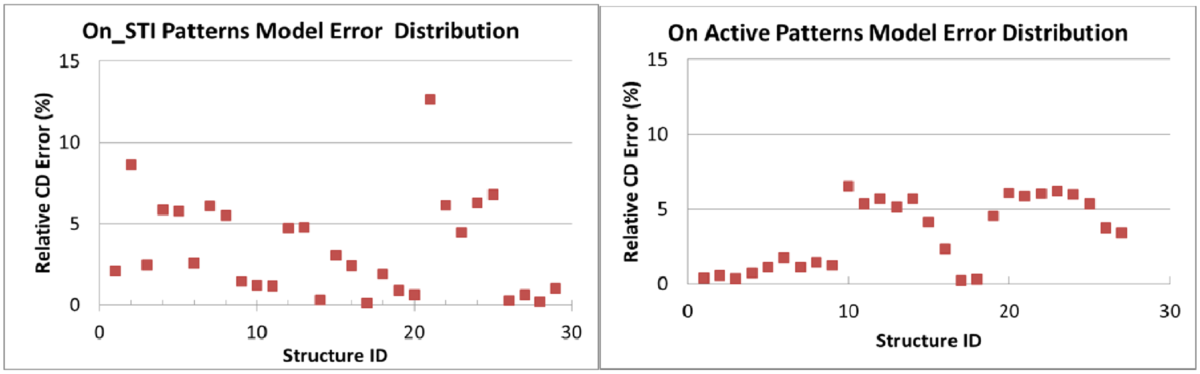


Fig 3 – Relative model error of patterns on planar substrate: left patterns on STI substrate and right patterns on Active substrate

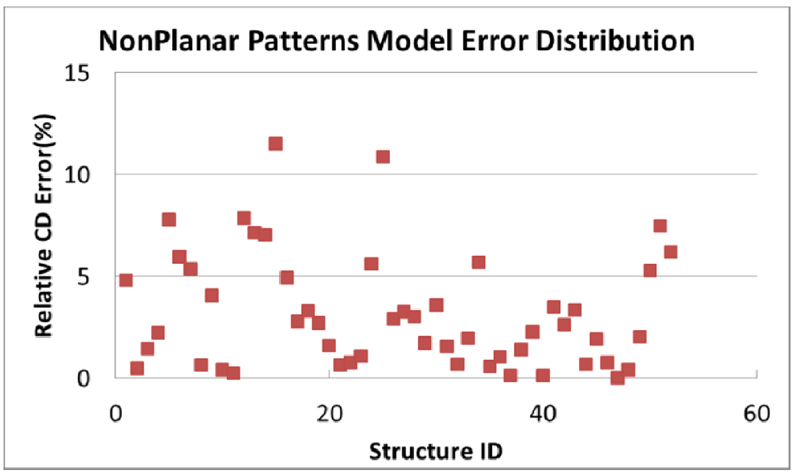


Fig 4 – Relative model error of patterns on non-planar substrate

The Poly model dataset integrate the patterns with two different substrates Poly on STI substrate and Poly on Active substrate. With the foundation of Active model, these two different substrates data is calibrated with poly-STI edge filter parameter and poly-active edge filter parameters. The poly data is well predicted with less than 10% relative model error for these two parts in Fig 5.

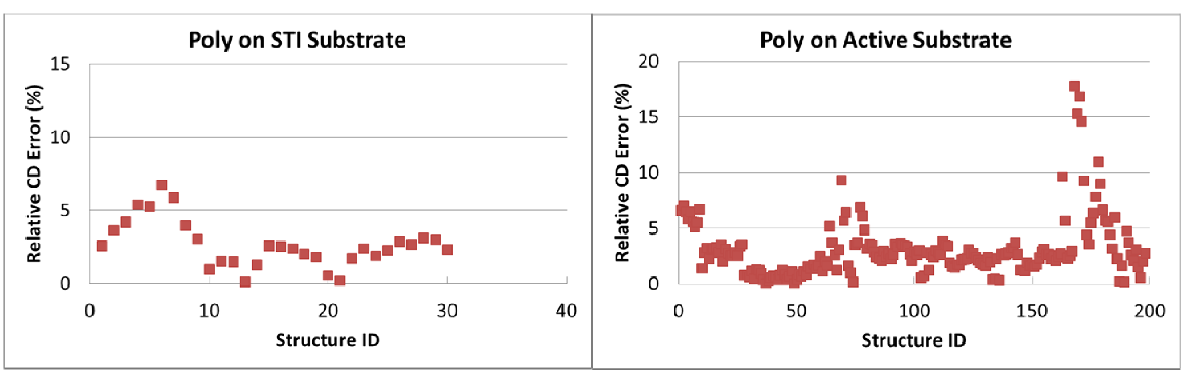


Fig 5 – Relative model error of patterns on Poly substrate: upper Poly on STI substrate and below Poly on Active substrate

4. MODEL VERIFICATION

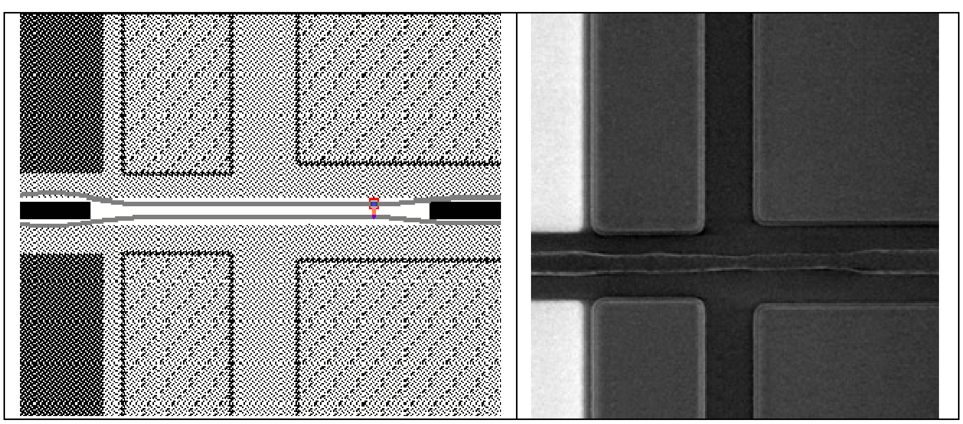
4.1 Wafer defectivity (PWQ)

To validate OPC model quality, full-chip mask verification has been correlated to defectivity on wafer. Design based defectivity on wafer is evaluated through a Process Window Qualification (PWQ) flow. The purpose of PWQ is to detect systematic defects on wafer and provide related process window. The PWQ flow is performed on a modulated wafer through lithography dose and focus parameters in order to stress patterning failure mechanism. The modulated wafer is scanned by a broad band optical signal which detects defects by die-to-die comparison on wafer. At end of wafer scanning, the detected defects are then sorted and filtered automatically through various defect parameters like defect size or brilliance and also defect pattern. As the detection is performed on a dose/focus modulated wafer, the resulting pattern based defect Pareto is able to deliver the process window for each pattern in the lithography dose & focus matrix. For each pattern, the dose/focus process window evaluated on wafer is then compared to the simulated process window in order to check OPC model accuracy. This flow has been exercised on a modulated wafer for implant source/drain layer at ADI step.

4.2 Model lithographical verification versus SEM images

Using Tachyon LMC (Lithography Manufacturing Check), weak points were highlighted in terms of strong wafer stack effects. Those hot spots were identified by the usage of appropriate implant detector settings on a full-chip verification run with off nominal exposure condition (60 nm defocus / -8% delta dose).

The hotspots selected below were typical hotspots reported by the LMC run in process window and observed on wafers. Figure 6 below is showing two hotspots examples comparing implant simulated contour with SEM images. The impact of the Active areas (black and dark grey regions) in term of reflection and contribution to the image intensity is clearly seen on the simulated contours as well as on the SEM images, even at nominal exposure condition.



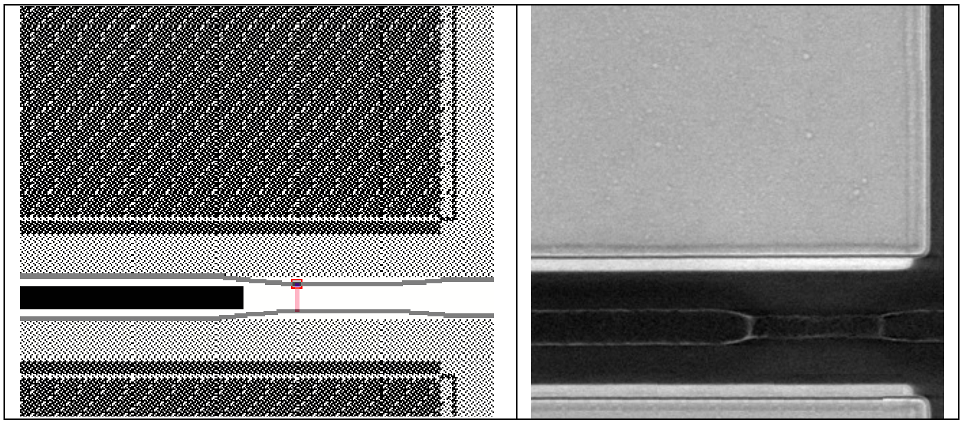


Fig 6 –Defects on Implant-Active distance at nominal exposure condition reported and confirmed on wafer (Active: black and dark grey areas)

The example on Figure 7 describes the behavior of a Bridging defect through Process Window. It strongly matches the SEM images at the same exposure conditions.

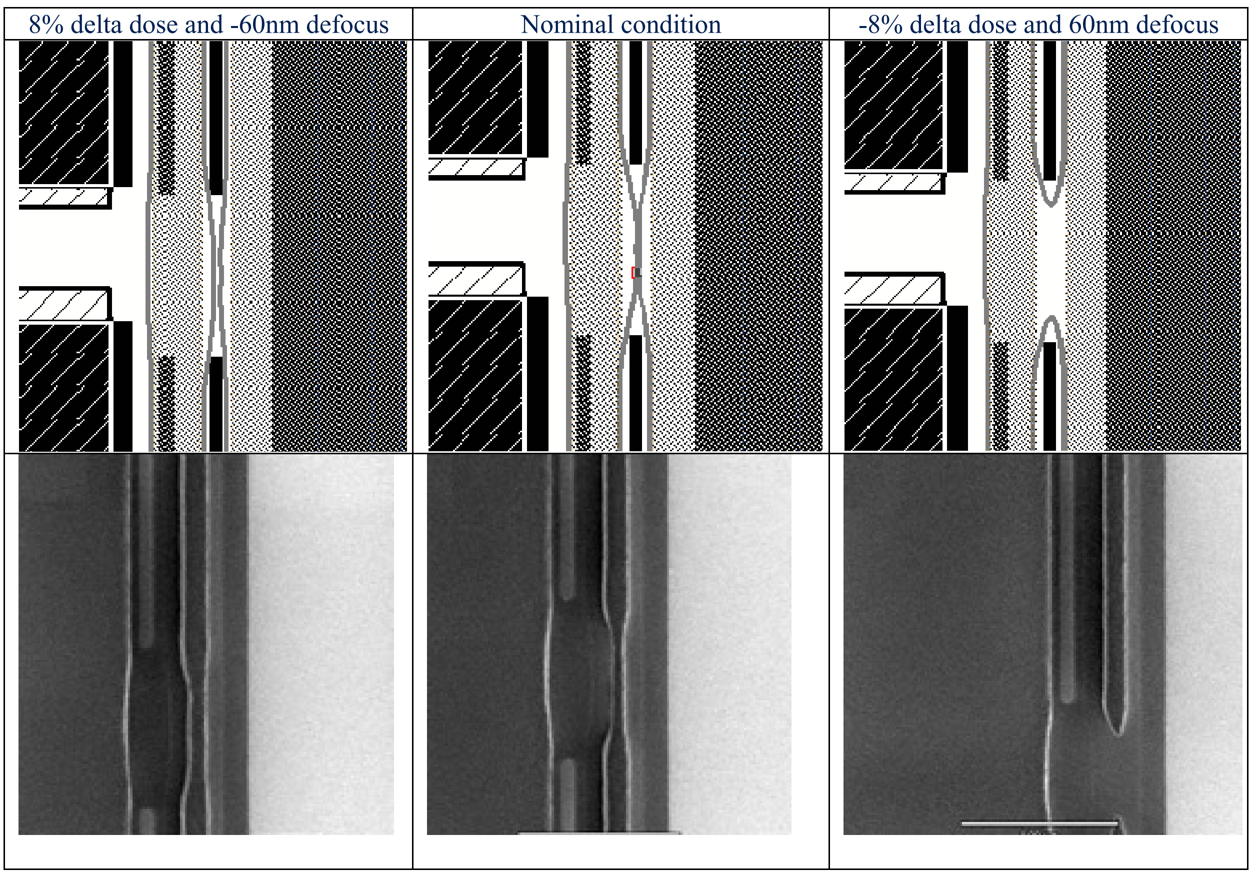


Fig 7 – Implant bridging defect through process window (Dark and dark grey=Active, hell grey = implant)

5. CONCLUSION

We have presented a full-chip model taking into account complex implant wafer stack effects. Those effects were caused by reflections coming from Active and Poly sub-layers. The W3D+ model is capable of successfully predicting lithographic behaviors observed on wafer which were not reported with a traditional single layer model.

The calibration methodology has been discussed and W3D+ model results were presented with modeling error less than 10% for 95% of calibration structures and less than 20% for rest of structures. Ultimate goal of this study was to perform a full-chip check through process window for implant layers using sub-layer reflections. In this work we demonstrated a good match between the W3D+ model prediction and wafer SEM images.

References:

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